# Midterm Examination I

EE 203 - Digital Systems DESIGN (Fall 2015)

MEF University

Assigned: November 3, 2015.
Due: at the end of class on November 3, 2015.
Instructor: Şuayb Ş. Arslan.

Name: _____

Student ID: _____

## Instructions

1. For every design you make or the solution you present, please show every step you take. I am looking for clear development of your approach for the solution so that you will be able to get partial credit.
2. This is a closed textbook exam. You **may not** work on the exam with anyone else, ask anyone questions, or consult the digital version of the textbook or other sites on the Web for answers.
3. You can use scratch paper and attach them to this hard-copy if you need more space.
4. Please make sure your hand writing is legible. Although you will not be penalised due to a potential disorganization in your submission, but it would be best if you can keep your solutions and paper organization at a certain quality.
5. Do not forget to staple or attach the pages of the hard copy you hand in.

I wish you the best of luck!

| Question # | 1 | 2 | 3 | 4 | Bonus | Total |
|---|---|---|---|---|---|---|
| Subject | Number Systems | Gates, Parity Coding and Multiplexers | Canonical forms/Karnough maps | Combinational Circuit Design | Decoders and Multiplexers | |
| Points | 25 | 25 | 20 | 30 | 10 | 100(+10) |
| | | | | | | |

**Problem 1** (Number Systems - **25 points**) Give appropriate answer to the following questions. Support your arguments.

1. The roots of the cubic equation $x^3 - 20x^2 + 115x - 140 = 0$ are given by $x = 3$, $x = 4$ and $x = 5$. What is the base of the numbers?
2. Let us have two decimal numbers $A = 49$ and $B = 26$. We would like to compute $B - A$ using binary number system and 2's complement. If we use a leading "1" to represent a negative binary number and "0" to represent a positive binary number, what is the final binary stream that represents $B - A$ in our digital system? How many bits at minimum you need to represent this binary number? Verify that your computation is valid by converting the binary number back to decimal number system.

**Problem 2** (Gates and Parity Coding - **25 points**) Give appropriate answer to the following questions. All the logic gates you use for this question must be two-input one-output.

1. Name one gate whose dual is also its complement.
2. Implement that gate using minimum number of NAND gates only. (Hint: For a correct answer, you will have to remember the identities such as $xx' = yy' = 0$ and DeMorgan's law.)
3. Implement the gate using a 2:1 multiplexer.
4. Using multiplexers, implement an even parity generator for 4 input bits. How many number of multiplexers you need? Draw the logic diagram. (Hint: Remember that an even parity generator generates a parity bit based on the 4-bit input such that the count of the total number of 1's in the parity added stream is even. Example: 1000**1**, where the last parity bit is added to make the total number of 1's even.)

**Problem 3** (Canonical forms/Karnough maps - **20 points**) Consider a 4 input function $F$. The minterm $X'Y'Z'T'$ is known to be in the SOP form of $F$.

1. What is the maximum number of minterms that the SOP form of $F$ can have such that no simplification is possible. Derive the corresponding Boolean expression for both SOP form and POS form. Can $F'$ be simplified?
2. Now suppose that all the other minterms that does not exist in the SOP form of $F$ are simply "don't care"s. Can the SOP expression of $F$ be simplified? If so, what is the simplified Boolean expression? What is $F'$?

**Problem 4** (Combinational Circuit Design - **30 points**) Consider a 4-input 3-output combinational circuit whose input/ouput relationships are expressed in terms of SOP form as follows:

$$F_0 = \sum\nolimits_m (4, 6, 7, 8, 10, 11) + \sum\nolimits_d (5, 9) \quad (1)$$

$$F_1 = \sum\nolimits_m (1, 3, 7, 13) + \sum\nolimits_d (5, 9) \quad (2)$$

$$F_2 = \sum\nolimits_m (0, 1, 2, 3, 7, 12, 13, 14, 15) + \sum\nolimits_d (5, 9) \quad (3)$$

Provide your answer for each of the following questions.

1. Draw Karnough maps for each output of the combinational circuit and apply minimization techniques by finding the essential and non-essential prime implicants.
2. Identify as many common terms as possible between the three simplified output expressions. Simplify the expressions by renaming the common terms.
3. Draw the final simplified logic diagram of the combinational circuit.
4. **(Bonus+10)** Can you implement $F_0$, $F_1$ using decoders (maybe with few more gates) and $F_2$ using multiplexers only (NOT gates are OK)? Explain your answer.