Final Examination

EE 203 - Digital Systems DESIGN (Fall 2015)

MEF University

Assigned: 12:00am on January 4, 2016.
Due: 1:50pm on January 4, 2016.
Location: A201, MEF University
Instructor: Şuayb Ş. Arslan.

Name: _____

Student ID: _____

Instructions

1. For every design you make or the solution you present, please show every step you take. I am looking for clear development of your approach for the solution so that you will be able to get partial credit.
2. This is a closed textbook exam. You **may not** work on the exam with anyone else, ask anyone questions, or consult the digital version of the textbook or other sites on the Web for answers.
3. Single-sided one page cheat sheet is allowed.
4. You can use scratch paper and attach them to this hard-copy if you need more space.
5. Please make sure your hand writing is legible. Although you will not be penalised due to a potential disorganization in your submission, but it would be best if you can keep your solutions and paper organization at a certain quality.
6. Do not forget to staple or attach the pages of the hard copy you hand in.

I wish you the best of luck!

Question #	1	2	3	4	5	6	7	8	Total
Subject	DNS G	CF M	COM DEC	SEQ	DCP C	SEQ C, KM	R, M	SCD	
Points	12	13	15	10	10	15(+5)	10(+5)	15	100(+10)

Acronyms:

- DNS: Digital and Number Systems, G: Gates,
- KM: Karnough Maps, DEC: Decoders,
- CF: Cannonical Forms, M: Multiplexers,
- COM: Combinational Circuits, SEQ: Sequential Circuits,
- DCP: Digital Circuit Primitives, C: Counters, R: Registers,
- SCD: Simple Computer Design.

Problem 1 (Digital and Number Systems, Gates - **12 points**) Please indicate whether the following statements are "True" or False".

1. There are two types of logic blocks: a. Combinational, b. Sequential. _____
2. The voltages or currents in digital electronics should be constantly varying. _____
3. In the unsigned binary number system, the maximum number that can be represented by $n-$bits is $2^n - 2$. _____
4. Conversion of the decimal number 151.75 to binary shall yield 11010011.01. _____
5. It is enough to use three bits to represent a BCD digit. _____
6. The odd *parity* bit for the code 111001 is 1. _____
7. If you subtract the binary number $Y = 0011001$ from $X = 0101110$, you will get 0010101. _____
8. The decimal value 125 has $6D$ hexadecimal equivalent. _____
9. In the signed binary number system, 101 and 11111101 can both be the representation of "-3" depending on how many bits we use to represent numbers. _____
10. In Gray coding, 101 can represent a bigger decimal number compared to what 111 can represent. _____
11. The number of Boolean functions that you can enamurate using n bits is 2^{2n}. _____
12. The dual of XNOR function/gate is also the complement of itself. _____

Problem 2 (Cannonical Forms, Multiplexers - **13 points**) Consider the following combinational circuit which has three inputs x, y, z and two outputs A and B.

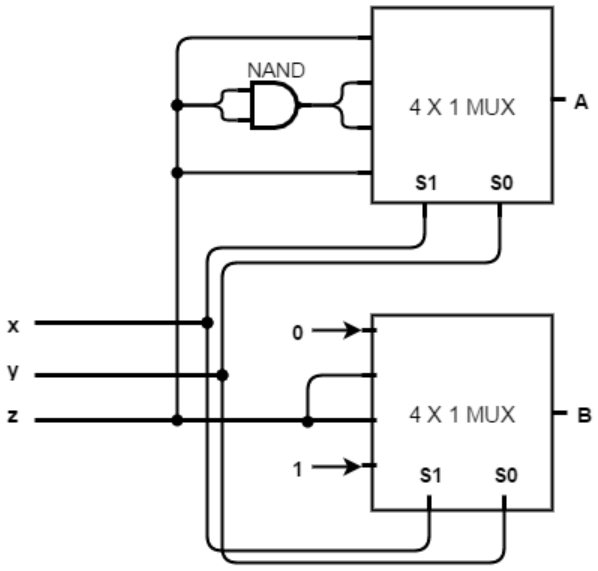


Figure 1: A combinational circuit using two 4×1 multiplexers.

1. Determine the outputs A and B in terms of x, y, z in both SOP and POS forms. How many terms do you have in each?
2. Draw the truth table and comment on the functionality of the circuit.

Problem 3 (Comparators, Conditionals, Decoders - **15 points**) In this question, we would like to implement conditional statements using decoders. Input variables X and Y are controlled by control variables S_0 and S_1. There are three outputs which are given by the following flow diagram.

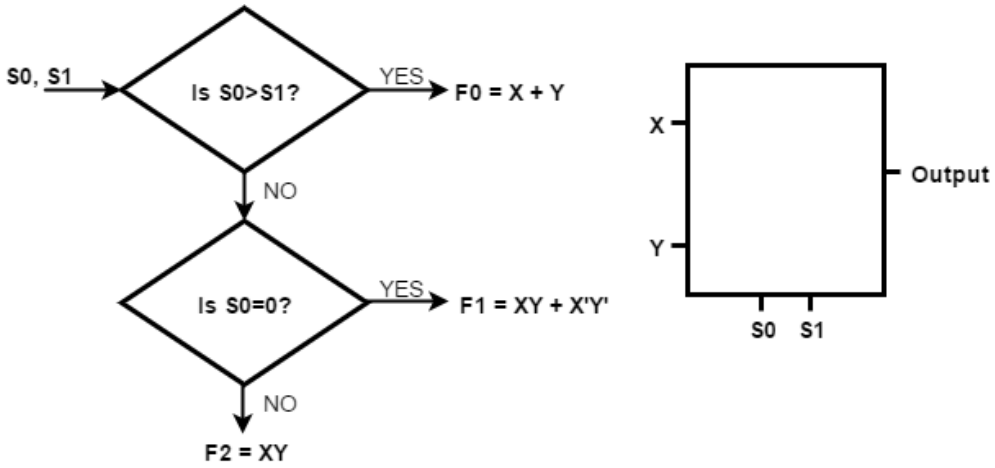
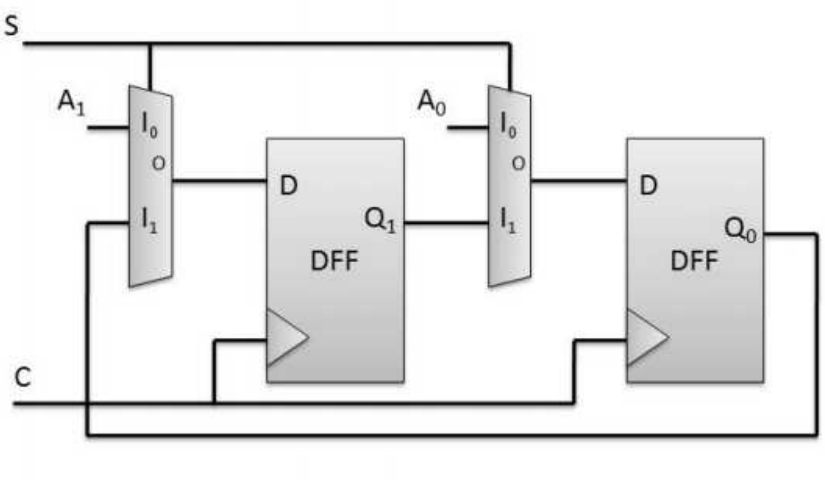


Figure 2: A conditional combinational circuit.

1. Design the combinational circuit that uses a decoder, a multiplexer and logic gates to perform the conditional logic illustrated above.
2. Draw the truth table for inputs X, Y, S_0, S_1 and outputs F_0, F_1 and F_2. Design the same combinational circuit using a decoder and logic gates.

Problem 4 (Sequential Circuit Timing Analysis - **10 points**) The below circuit shows a sequential circuit that uses two D-flipflops and two multiplexers. There are three inputs to the circuit, namely A_0, A_1 and S. The input C is the clock and the state variables Q_1 and Q_0 are the output of the circuit. At time t_0, the output values $Q_1 = 0$ and $Q_0 = 1$. Show the timing diagram for the state variables Q_1 and Q_0 in the space provided below.



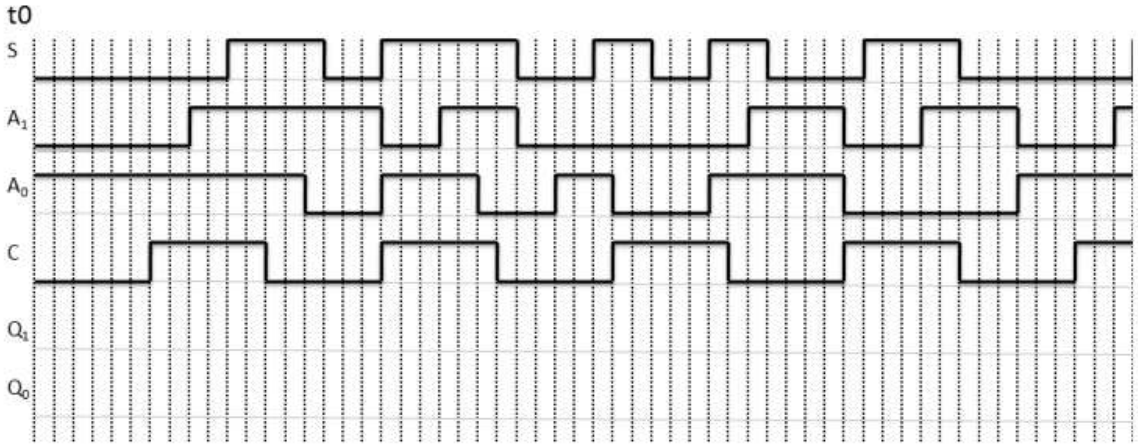


Figure 3: The timing diagram for the sequential circuit shown above.

Problem 5 (Digital Circuit Primitives, Counters - **10 points**) Please circle one of the answers provided for the following questions below.

1. In general, which of the following machines have simpler logic?

   a. Moore b. Mealy

2. In contrast to a binary counter, how many extra flipflops does a ring counter use if both counters can count from 0 to 27?

   a. 22 b. 23 c. 24 d. 25

3. In contrast to a binary counter, how many extra flipflops does a Johnson counter use if both counters can count from 0 to 27?

   a. 6 b. 7 c. 8 d. 9

4. Which sequential circuit is faster?

   a. Latches b. Flipflops

5. For a sequential sequence detector which is designed to detect the bit pattern "10101", how many states at minimum should we have in its state diagram representation?

   a. 3 b. 4 c. 5 d. 6

Problem 6 (Sequential Circuit Design, Counters, Karnough Maps - **15 points**) We would like to design a 2-bit binary up/down counter. If the input x is 1 the counter counts up and if x is 0, the counter counts down. An example input and the corresponding decimal equivalent of the counter is given by

$$\begin{aligned} x &: \quad 1\,1\,1\,1\,1\,1\,1\,1\,1\,1\,0\,0\,0\,0\,1 \ \ldots \\ \textit{counter} &: \quad 0\,1\,2\,3\,0\,1\,2\,3\,0\,1\,2\,1\,0\,3\,2\,3 \ \ldots \end{aligned}$$

Please design the up/down counter using JK flipflops. Use as few gates as possible in your design. (**Bonus +5**) Add an enable (**EN**) input to your circuit so that if the enable is de-asserted, the counter stops counting.

Problem 7 (Registers, Multiplexers - **10 points**) We would like to design a 4-bit register with the following specifications.

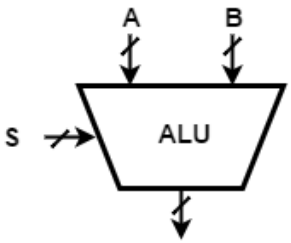
- The register is supposed to have four modes of operation given by the following table. It has two control inputs $\mathbf{s_0}$ and $\mathbf{s_1}$.

$\mathbf{s_0}$	$\mathbf{s_1}$	**Operation**
0	0	Unchanged
0	1	Complement of the output
1	0	Clear (set register's contents to 0)
1	1	Load parallel data

- Use JK flipflops and multiplexer/s.
  (**Bonus +5**) What does it take in the design to change "Complement of the output" to "2's complement of the output" ?

Problem 8 (Simple Computer Design - **15 points**) We would like to design a simple 8-bit multi-cycle computer with the following components:

- A single data operand register, DR
- A 64×8 i.e., $6-$bit addressable Read-Only-Memory, ROM
- An 8-bit instruction register, IR
- A two input $8-$bit ALU with two bits of control based on following definition table:



a) High level block diagram for ALU

Select	Operations
00	A ADD B
01	A ADD 1
10	A NAND B
11	NOT A

b) Operations by ALU

c) Instruction format

Figure 4: The ALU for the simple computer.

The instructions are $8-$bit long with two bits reserved for opcode (OP) and six bits for the ROM address information. We assume three instructions to perform three operations, namely binary addition (ADD), subtraction (SUB) and NOR, corresponding to the opcodes 00, 01, 11, respectively. They work as follows:

$$\text{DR} \leftarrow \text{DR } OP \text{ ROM[ADDR]} \tag{-3}$$

Draw a simple Datapath to execute these instructions. Please clearly label all the control signals. Note that you do not need to design the internal details of ALU, ROM, registers and the PC. In your Datapath, you can use encoders, decoders, multiplexers and demultiplexers as much as you need.